

FIG. 1

BLOCK DIAGRAM SHOWING CONSTRUCTION OF FIRST EMBODIMENT

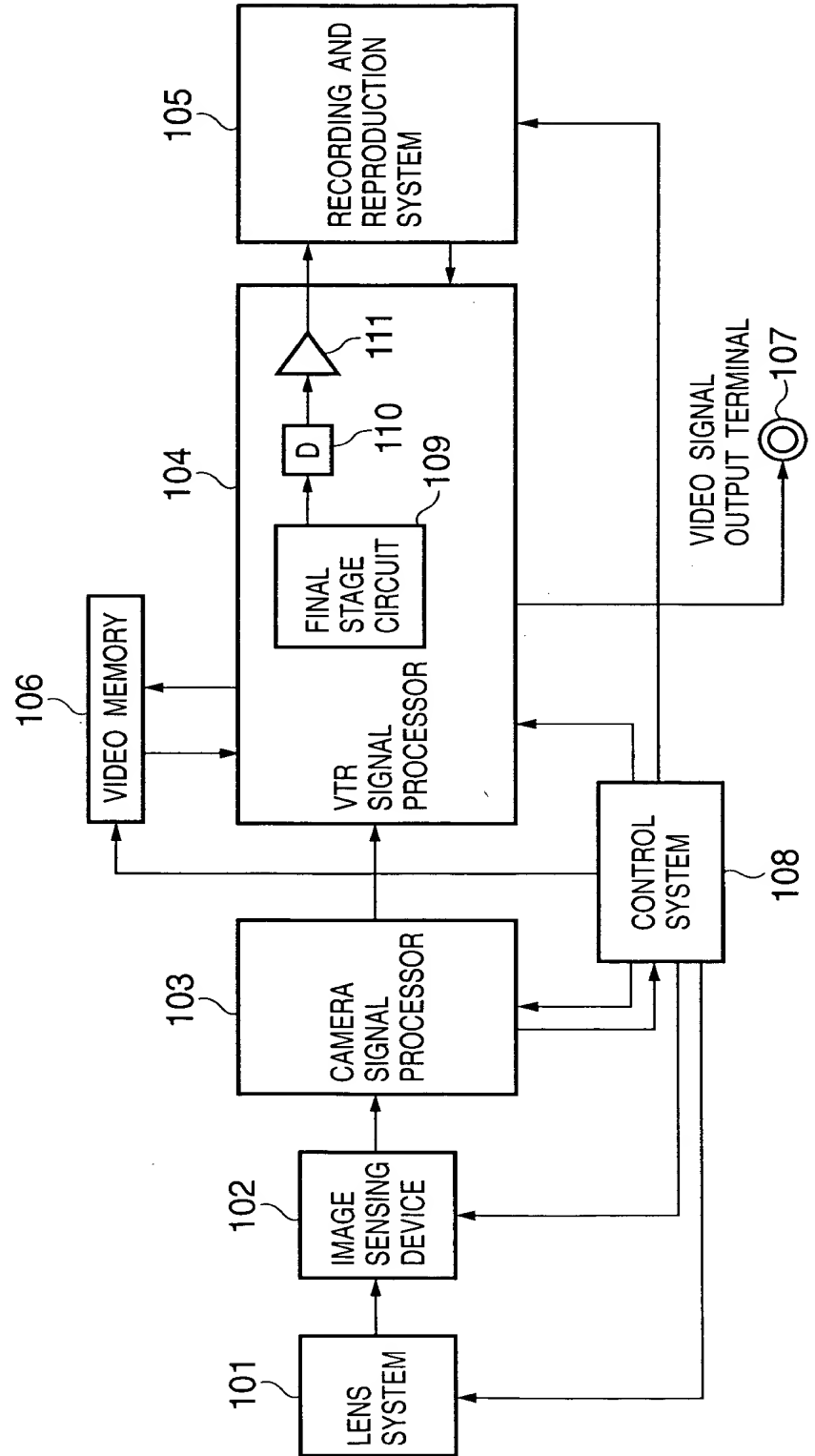
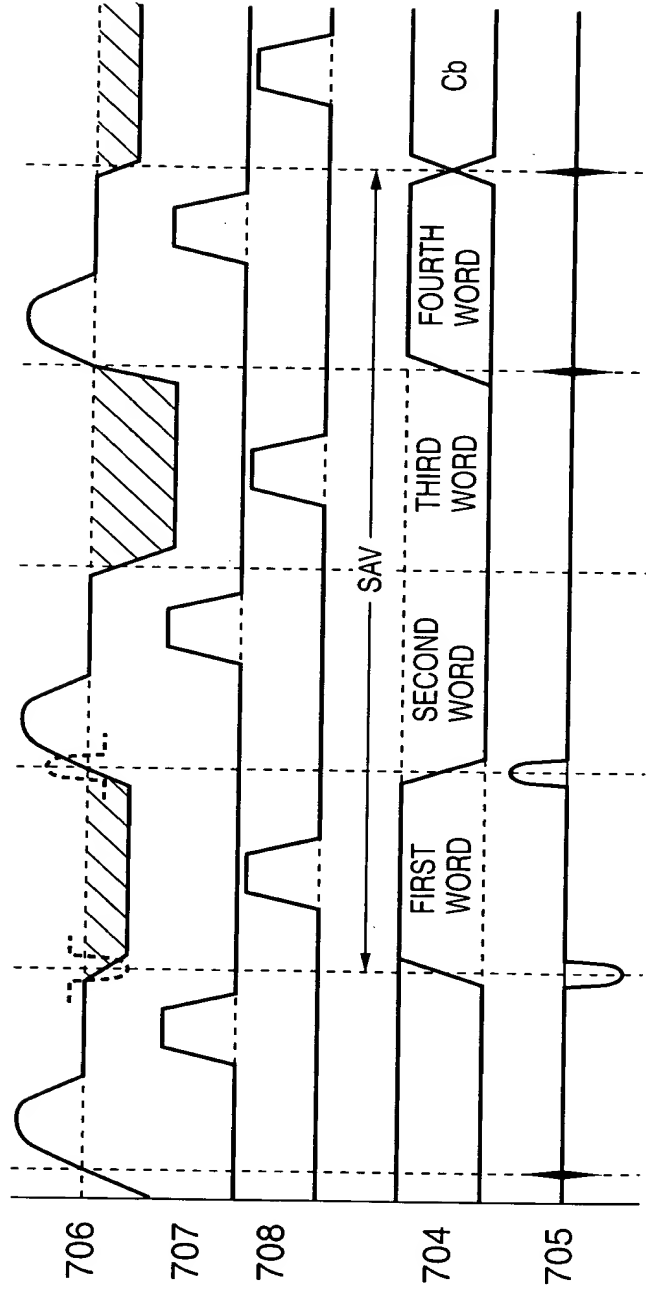


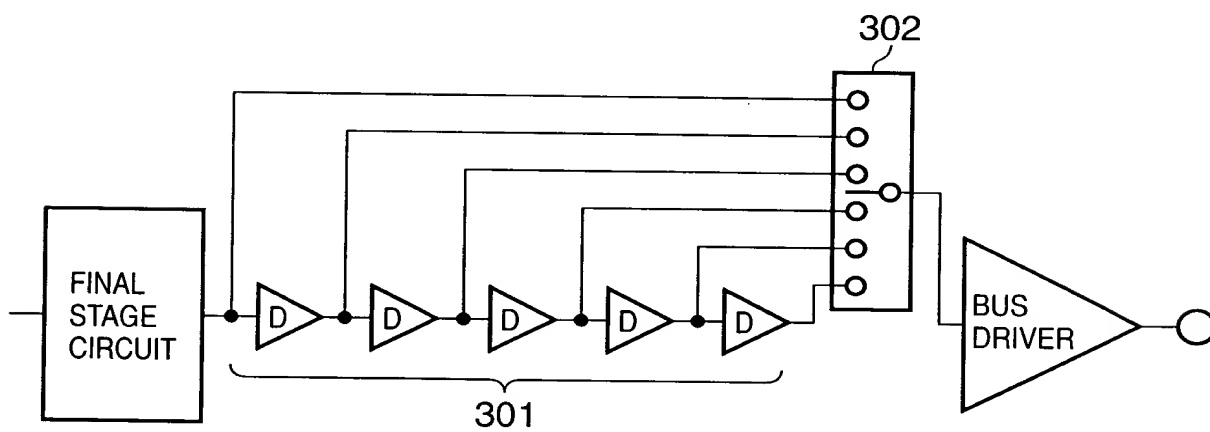
FIG. 2

TIMING CHART SHOWING OPERATION OF FIRST EMBODIMENT



**FIG. 3**

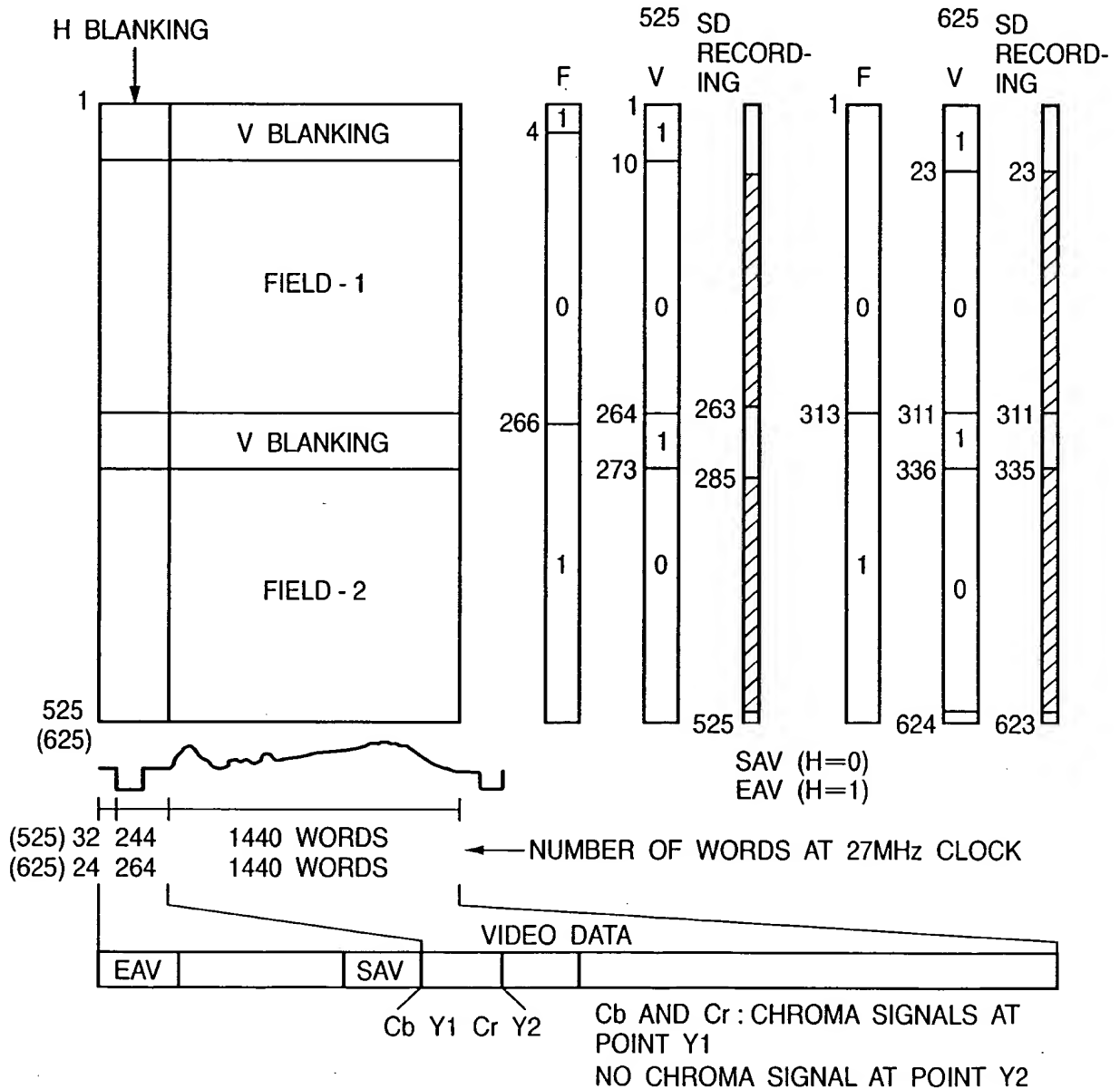
DIAGRAM SHOWING DELAY CIRCUIT IN SECOND EMBODIMENT



# FIG. 4

## EXPLANATORY VIEW OF RECORDING FORMAT CCIR Rec 601

4:2:2:1/F (IN CONFORMITY WITH CCIR Rec 601 / SMPTE 125M)



# FIG. 5

## EXPLANATORY VIEW OF RECORDING FORMAT CCIR Rec 601

### CONTENTS OF EAV, SAV

	MSB	6	5	4	3	2	1	LSB	F	V	H	P3	P2	P1	P0
FIRST WORD	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0
SECOND WORD	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1
THIRD WORD	0	0	0	0	0	0	0	0	0	1	0	1	0	1	1
FOURTH WORD	1	F	V	H	P3	P2	P1	P0	0	1	1	0	1	1	0
									1	0	0	0	1	1	1
									1	1	0	1	1	0	0
									1	1	1	0	0	0	1

00h AND ffh ARE NOT USED IN VIDEO DATA

10h (PEDESTAL LEVEL) IS USED IN OTHER POSITIONS THAN SAV AND EAV (BLANKING)

80h IS USED IN POSITIONS OF Cb AND Cr

SAV AND EAV EXIST IN ALL LINES (ALSO IN V BLANKING)

PARITY IS ALWAYS ADDED ON TRANSMITTING SIDE, AND USED ARBITRARILY ON RECEIVING SIDE

**FIG. 6**

SCHEMATIC DIAGRAM SHOWING NOISE OCCURRENCE  
POSITION IN CONVENTIONAL ART

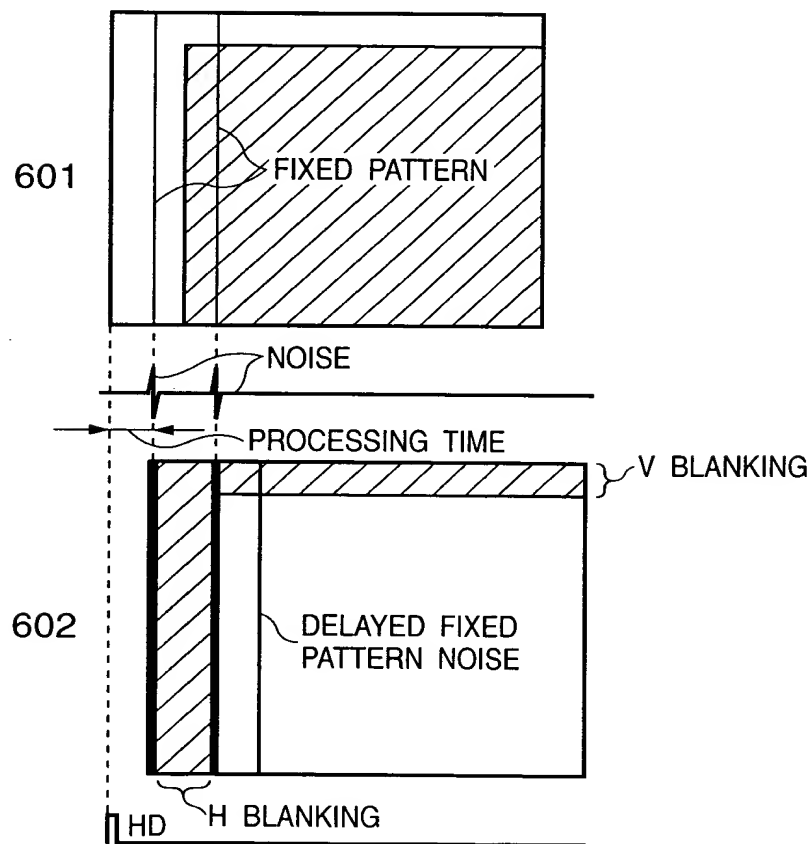
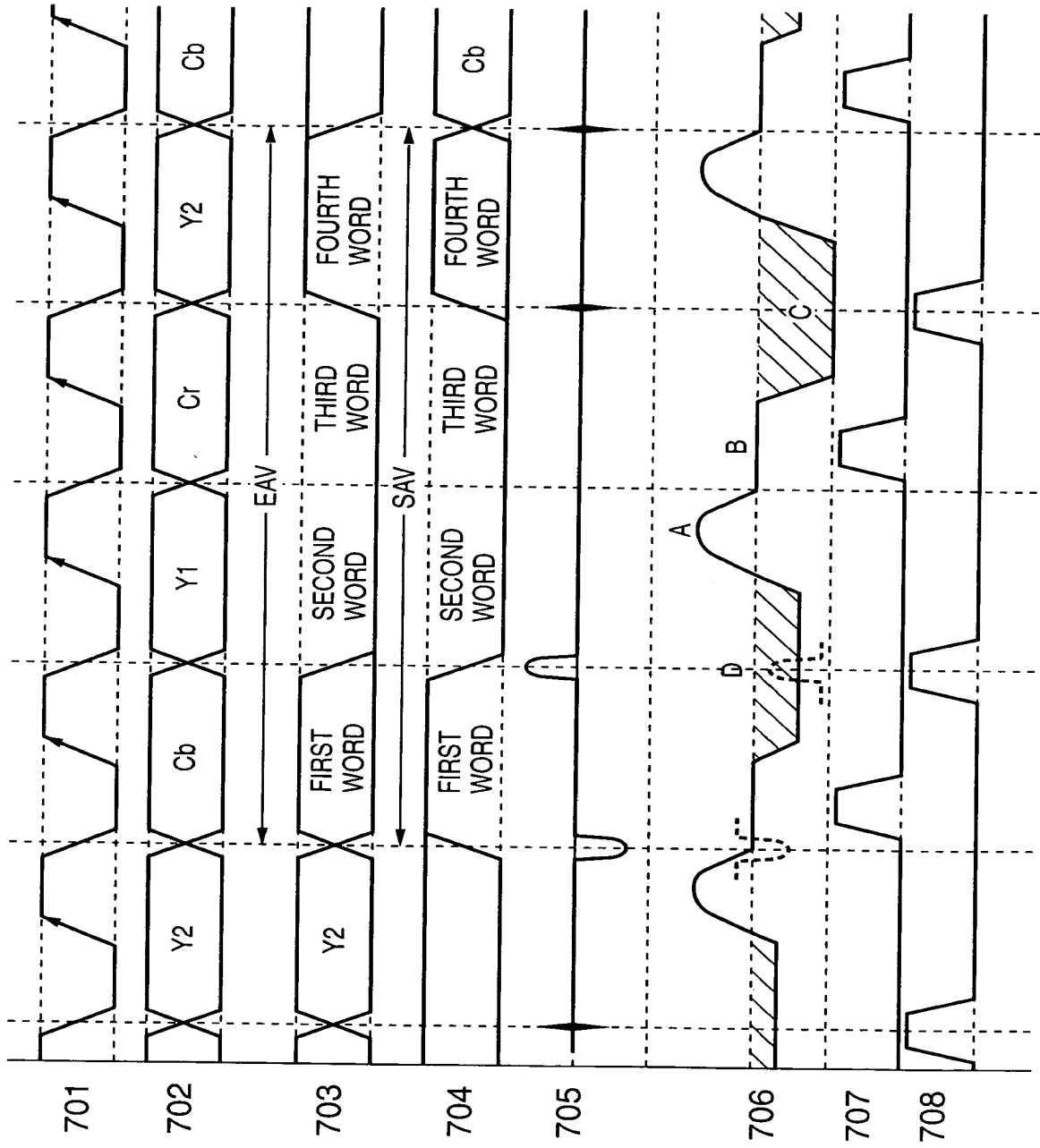


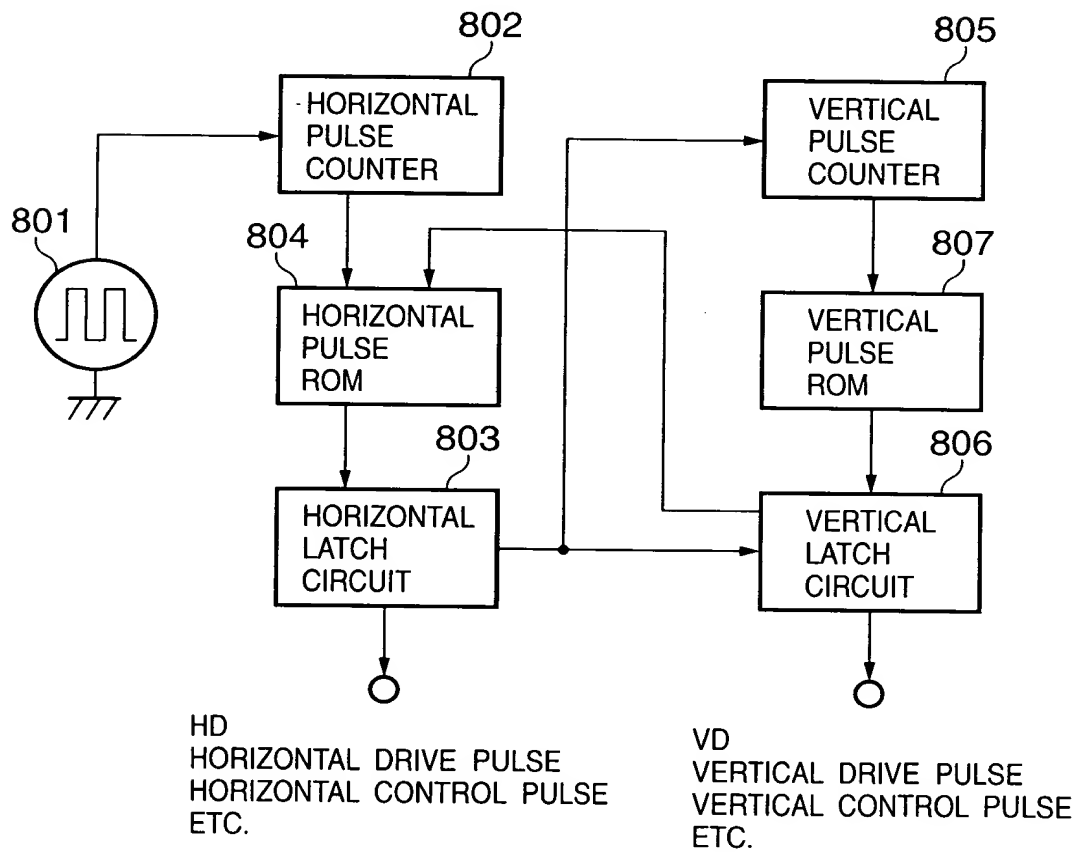
FIG. 7

TIMING CHART SHOWING OCCURRENCE AND MIXING OF NOISE



# FIG. 8

BLOCK DIAGRAM SHOWING CONSTRUCTION OF CIRCUIT TO GENERATE SYNCHRONIZING SIGNALS AND CONTROL SIGNALS



**FIG. 9**

BLOCK DIAGRAM SHOWING ARRANGEMENT OF PROCESSING FINAL STAGE AND  
PARALLEL BUS DRIVE CIRCUIT IN VTR SIGNAL PROCESSOR

